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#6	(memory coherency<IN>metadata)
#7	adder or (adding unit)
#8	bank size
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#10	(((multiple bank*)<in>metadata)) <AND> ((multiple tower*<IN>metadata))
#11	((multiple tower*<IN>metadata)) <AND> ((memory or bank) and interleav*)
#12	((memory coherency<IN>metadata)) <AND> (bank size)
#13	((aligner or alignment unit<IN>metadata)) <AND> (bank size)
#14	(((aligner or alignment unit<IN>metadata)) <AND> (bank size)) <AND> ((memory or bank) and interleav*)

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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S3	8296	first adj2 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:25
S4	7351	second adj2 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:26
S5	392	size near3 ("same" or equal$4) near5 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:27
S6	10694	first adj2 adder	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:27
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S8	467	second adj row adj address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:28
S9	847	first adj row adj address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:28

EAST Search History

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S11	386	S8 and S9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:28
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S47	1560	S43 and S44 and S45	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 10:47
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S53	2297826	se	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 10:48
S54	5708735	segment$2 or line$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 10:48
S55	790789	segment$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 10:49
S56	6	S52 and S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/29 10:49

Terms used
memory bank interleav simultaneous unaligned adder memory row address

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1 A survey of commercial parallel processors

Edward Gehringer, Janne Abullarade, Michael H. Gulyn

September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4

Publisher: ACM Press

Full text available: pdf(2.96 MB) Additional Information: full citation, abstract, citings, index terms

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share ...

Terms used
memory alignment multiported memory bank simultaneous access

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1 Performance of the vectorial processor VEC-SM2 using serial multiport memory

J. Jorda, A. Mzoughi, O. Lafontaine, D. Litaize
January 1996 **Proceedings of the 10th international conference on Supercomputing**
Publisher: ACM Press
Full text available: pdf(777.69 KB) Additional Information: full citation, references, index terms

2 Data and memory optimization techniques for embedded systems

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsberg
April 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 2
Publisher: ACM Press
Full text available: pdf(339.91 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizations in embedded systems. The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipation of the resulting implementation. We first examine architecture-independent optimizations in the form of code transoformations. We next cover a broad spectrum of optimizati ...

Keywords: DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data cache, data optimization, high-level synthesis, memory architecture customization, memory power dissipation, register file, size estimation, survey

3 On-chip vs. off-chip memory: the data partitioning problem in embedded processor-based systems

Preeti Ranjan Panda, Nikil D. Dutt, Alexandru Nicolau
July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3
Publisher: ACM Press
Full text available: pdf(175.91 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Efficient utilization of on-chip memory space is extremely important in modern embedded system applications based on processor cores. In addition to a data cache that interfaces with slower off-chip memory, a fast on-chip SRAM, called Scratch-Pad memory, is often used in several applications, so that critical data can be stored there with a guaranteed fast access time. We present a technique for efficiently exploiting on-chip Scratch-Pad memory by partitioning the application's scalar and a ...

Keywords: data cache, data partitioning, memory synthesis, on-chip memory, scratch-pad memory, system design, system synthesis

4 A conflict-free memory design for multiprocessors

Honda Shing, Lionel M. Ni
August 1991 **Proceedings of the 1991 ACM/IEEE conference on Supercomputing**
Publisher: ACM Press
Full text available: pdf(1.21 MB) Additional Information: full citation, references, citings, index terms

5 High-bandwidth address translation for multiple-issue processors

Todd M. Austin, Gurindar S. Sohi
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2
Publisher: ACM Press
Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, references, citings, index terms

In an effort to push the envelope of system performance, microprocessor designs are continually exploiting higher levels of instruction-level parallelism, resulting in increasing bandwidth demands on the address translation mechanism. Most current microprocessor designs meet this demand with a multi-ported TLB. While this design provides an excellent hit rate at each port, its access latency and area grow very quickly as the number of ports is increased. As bandwidth demands continue to increase ...

6 A cost effective architecture for vectorizable numerical and multimedia applications

Francisca Quintana, Jesus Corbal, Roger Espasa, Mateo Valero
July 2001 **Proceedings of the thirteenth annual ACM symposium on Parallel algorithms and architectures**
Publisher: ACM Press
Full text available: pdf(293.82 KB) Additional Information: full citation, abstract, references, index terms

This paper analyzes the performance of vector-dominated regions of code in numerical and multimedia applications in a superscalar+vector architecture and compares it to an 8-way superscalar processor. The ability to split a program's execution into scalar and vector regions allows us to show that (1) as expected, the vector unit is much better than the wide issue superscalar at executing the vector-dominated regions of the code; (2) on the scalar regions, the 8-way superscalar, although bette ...

7 A VLIW architecture for a trace scheduling compiler

Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman
October 1987 **ACM SIGARCH Computer Architecture News , ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the second international conference on Architectual support for programming languages and operating systems ASPLOS-II**, Volume 15 , 22 , 21 Issue 5 , 10 , 4
Publisher: IEEE Computer Society Press, ACM Press
Additional Information: full citation, abstract, references, citings, index

Full text available: pdf(1.59 MB) terms

Very Long Instruction Word (VLIW) architectures were promised to deliver far more than the factor of two or three that current architectures achieve from overlapped execution. Using a new type of compiler which compacts ordinary sequential code into long instruction words, a VLIW machine was expected to provide from ten to thirty times the performance of a more conventional machine built of the same implementation technology.Multiflow Computer, Inc., has now built a VLIW called the TRACE™< ...

8 High-performance multi-queue buffers for VLSI communications switches

Y. Tamir, G. L. Frazier

May 1988 **ACM SIGARCH Computer Architecture News , Proceedings of the 15th Annual International Symposium on Computer architecture ISCA '88**, Volume 16 Issue 2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.41 MB) Additional Information: full citation, abstract, references, citings, index terms

Small nxn switches are key components of multistage interconnection networks used in multiprocessors as well as in the communication coprocessors used in multicomputers. The design of the internal buffers in these switches is of critical importance for achieving high throughput low latency communication. We discuss several buffer structures and compare them in terms of implementation complexity and their ability to deal with variations in traffic patterns a ...

9 Probabilistic analysis of a crossbar switch

T. N. Mudge, B. A. Makrucki

April 1982 **Proceedings of the 9th annual symposium on Computer Architecture**

Publisher: IEEE Computer Society Press

Full text available: pdf(772.83 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a probabilistic analysis of a crossbar switch interconnection network. A crossbar switch can be used to interconnect various combinations of computer subsystems. In the analysis below it is assumed, without loss of generality, that the crossbar is being used to connect N processors to M memories. The crossbar is termed an N-M crossbar (read "N to M crossbar"). General expressions are developed for a variety of performance fig ...

10 Half-price architecture

Ilhyun Kim, Mikko H. Lipasti

May 2003 **ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture ISCA '03**, Volume 31 Issue 2

Publisher: ACM Press

Full text available: pdf(278.61 KB) Additional Information: full citation, abstract, references, citings

Current-generation microprocessors are designed to process instructions with one and two source operands at equal cost. Handling two source operands requires multiple ports for each instruction in structures--such as the register file and wakeup logic--which are often in the processor's critical timing paths. We argue that these structures are overdesigned since only a small fraction of instructions require two source operands to be processed simultaneously. In this paper, we propose the half-pr ...

11 Design space exploration for 3D architectures

Yuan Xie, Gabriel H. Loh, Bryan Black, Kerry Bernstein

April 2006 **ACM Journal on Emerging Technologies in Computing Systems (JETC)**, Volume 2 Issue 2

Publisher: ACM Press

Full text available: pdf(1.93 MB) Additional Information: full citation, abstract, references, index terms

As technology scales, interconnects have become a major performance bottleneck and a major source of power consumption for microprocessors. Increasing interconnect costs make it necessary to consider alternate ways of building modern microprocessors. One promising option is 3D architectures where a stack of multiple device layers with direct vertical tunneling through them are put together on the same chip. As fabrication of 3D integrated circuits has become viable, developing CAD tools and arch ...

Keywords: 3D integration, hardware, microarchitecture, processor architectures

12 Trace cache: a low latency approach to high bandwidth instruction fetching

Eric Rotenberg, Steve Bennett, James E. Smith

December 1996 **Proceedings of the 29th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings, index terms

As the issue width of superscalar processors is increased, instruction fetch bandwidth requirements will also increase. It will become necessary to fetch multiple basic blocks per cycle. Conventional instruction caches hinder this effort because long instruction sequences are not always in contiguous cache locations. We propose supplementing the conventional instruction cache with a trace cache. This structure caches traces of the dynamic instruction stream, so instructions that are otherwise no ...

Keywords: instruction cache, instruction fetching, multiple branch prediction, superscalar processors, trace cache

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